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GB-A- 2 113 910

IEEE ELECTRON DEVICE LETTERS, vol. EDL-5, no. 5, May 1984, pages 151-153, IEEE, New York, US; J.C. STURM et al.: "A three-dimensional folded dynamic RAM in beam-recrystallized polysilicon"

PATENT ABSTRACTS OF JAPAN, vol. 9, no. 43 (E-298)[1766], 22nd February 1985 & JP-A-59-181 555

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of the memory cells has a conventional structure and is formed in the substrate outside the well region. V_{CC} (0 V) or a minus voltage can be adopted for the substrate voltage as usual, which ensures a stable performance of the peripheral circuit.

Particular examples of semiconductor memory devices in accordance with this invention will now be described with reference to the accompanying drawings; in which:-

Figures 1A is a partial section through a first example of memory cell of a DRAM device;

Figure 1B is a partial plan of the first example;

Figure 2 is a partial section through a second example of a memory cell of a DRAM device;

Figure 3A is a partial section through a third example of a memory cell of a DRAM device;

Figure 3B is a partial sectional view of an FET of a peripheral circuit of the third example of a DRAM device; and,

Figure 3C is a partial section through a modification of the third example of memory cell.

Referring to Figures 1A and 1B, a DRAM device according to the present invention comprises memory cells, each of which is composed of an FET and a trench-capacitor.

In the drawings, a semiconductor substrate 1 is, for example, an n-type silicon single crystalline substrate, and has a V-groove 2 for the trench-capacitor. An insulating layer 3 of, e.g., silicon dioxide (SiO_2), is formed on the substrate 1 and consists of a thick portion 3a and a thin portion 3b. A semiconductor layer 4 of, e.g., polycrystalline silicon, is formed on the insulating layer 3.

A gate insulating layer 5 of, e.g., SiO_2, and a gate electrode 6 of, e.g., polycrystalline silicon, (i.e., a word line) are formed on the semiconductor layer 4 above the thick insulating layer portion 3b. The FET is composed of the gate insulating layer 5, the gate electrode 6, an n-type source region 4s, an n-type drain region 4d, and a p-type channel region 4c. These regions 4s, 4d, and 4c are formed in the semiconductor layer 4. Thus, the FET has the SOI structure. The trench-capacitor is composed of a dielectric (insulation) layer of the thin semiconductor layer portion 3b, an upper capacitor electrode of the portion of the semiconductor layer 4, and a lower capacitor electrode of the substrate 1. The electric charge for information is stored in the thin insulating layer portion 3b. An insulating layer 7 of, e.g., SiO_2 is formed over the entire surface and has a contact hole 8 wherein a portion of the source region 4s is exposed. In Fig. 1B the layer 7 is omitted. A conductive layer 9 of, e.g., aluminum (i.e., a bit line) is formed on the insulating layer 7 and is connected with the source region 4s.

In the memory cell having the above-mentioned structure, since the FET is isolated from the substrate 1, the substrate 1 can be biased with a suitable (intermediate) voltage for the capacitor between a first storage voltage (practically the supply voltage V_{CC} of, e.g., 5 V) for high level information, and a second storage voltage (practically, the ground voltage of 0 V) for low level information. For example, where V_{CC} is +5 V, it is preferable to bias the substrate 1 with +2.5 V, i.e., 1/2 V_{CC}. Accordingly, the capacitor is supplied with 2.5 V. In a conventional memory device, since a substrate is usually biased with the ground voltage or a minus voltage of from -2 to -3 V, a capacitor is supplied with a voltage of 5 V or 7 to 8 V. Thus compared with the conventional device, it is possible to substantially decrease an electric field strength in the dielectric layer of the capacitor.

FETs of a peripheral circuit of a memory device may have the SOI structure and be formed by using the polycrystalline silicon layer 4 on the thick SiO_2 layer 3a.

The memory device of Figs. 1A and 1B is produced in the following manner.

An n-type single crystalline silicon substrate 1 is thermally oxidized to form a thick SiO_2 layer 3a. The SiO_2 layer 3a is selectively etched to expose a portion of the substrate 1. The exposed portion is anisotropically etched to form a V-groove 2 or a U-groove. The substrate 1 is thermally oxidized to form a thin SiO_2 layer 3b on the groove surface. Then, a p-type polycrystalline silicon layer 4 is deposited over the entire surface by a chemical vapor deposition (CVD) method and is patterned by an etching method. In order to form a thin SiO_2 layer including a gate insulating layer 5 on the polycrystalline silicon layer 4, a thermal oxidation treatment is carried out. A polycrystalline silicon layer is formed over the exposed surface by a CVD method and is then selectively etched to form a word line 6 including a gate electrode. Donor impurities (e.g., phosphorous) are implanted in the polycrystalline silicon layer 4 by an ion-implantation method to form an n-type source region 4s and an n-type drain region 4d. An SiO_2 layer 7 is then formed over the entire surface and is selectively etched to form a contact hole 8. An aluminum layer is formed on the SiO_2 layer 7 and is patterned by etching to form a bit line 9 connecting with the n-type source region 4s. Thus the memory cell having the FET and the trench-capacitor is obtained, as shown in Fig. 1A.

A memory device according to another embodiment of the present invention is illustrated in Fig. 2. In this case, a semiconductor layer 4 is of a single crystalline silicon and the V-groove is filled with a polycrystalline silicon filler 21. In Fig. 2, the same reference numerals as those shown in Figs. 1A and 1B indicate the same portions.

The device is produced in a similar manner to

capacitor (3b, 4, 32), formed in a well region (32) of second conductivity type, opposite the first conductivity type, in a surface portion of the semiconductor substrate (31);

an insulating layer having a thin portion (3b) and a thick portion (41) formed on the well region (32);

a semiconductor layer (4) formed on the insulating layer (41, 42); and the memory cell field effect transistor (4s, 4c, 4d) being formed in the semiconductor layer (4); and,

the memory cell capacitor having its dielectric formed by the thin portion (3b) of the insulating layer, an upper electrode of the second conductivity type formed by a portion of the semiconductor layer (4), and a lower electrode formed by the well portion (32); the well portion being arranged to be biased with a voltage at an intermediate level between a first storage voltage and a second storage voltage applied to the semiconductor layer, thereby reducing the field strength across the dielectric of the memory cell capacitor.

2. A semiconductor memory device according to claim 1, wherein the field effect transistor comprises a source region (4s) and a drain region (4d) formed in the semiconductor layer (4) and a gate electrode (6) formed on a gate insulating layer (5) formed on the semiconductor layer (4).

3. A semiconductor memory device according to claim 1 to 2, wherein the capacitor is a trench type capacitor.

4. A semiconductor memory device according to claim 3, wherein the semiconductor layer is composed of a polycrystalline silicon portion (21) filling the trench and a single crystalline silicon portion (4) formed on the polycrystalline silicon portion (21) and on the insulating layer (3a)(Figure 2).

5. A semiconductor memory device according to claim 1 or 2, wherein the semiconductor layer is formed entirely of poly-crystalline silicon.

6. A semiconductor memory device according to any one of claims 1 or 2, wherein the semiconductor layer is formed entirely of single crystal silicon.

7. A semiconductor memory device according to any one of the preceding claims, wherein the first storage voltage is a supply voltage and the second storage voltage is ground voltage.

8. A semiconductor memory device according to claim 7, wherein the intermediate level voltage is half the supply voltage.

Revendications

1. Dispositif de mémoire semiconducteur comprenant :

un circuit périphérique composé d'un transistor à effet de champ (34d, 34s, 36) formé dans un substrat semiconducteur (31) d'un premier type de conductivité et une cellule mémoire composée d'un transistor à effet de champ (4s, 4c, 4d) et d'une capacité (3b, 4, 32), formée dans une région de caisson (32) du second type de conductivité opposé au premier type de conductivité, dans une partie de surface du substrat semiconducteur (31) ;

une couche d'isolation comprenant une partie mince (3b) et une partie épaisse (41) formée dans la région de caisson (32) ;

une couche de semiconducteur (4) formée sur la couche d'isolation (41, 42) ; le transistor à effet de champ (4s, 4c, 4d) de la cellule mémoire étant formé dans la couche de semiconducteur (4) ;

la capacité de la cellule mémoire ayant son diélectrique formé par la partie mince (3b) de la couche d'isolation, par une électrode supérieure du second type de conductivité formée par une partie de la couche de semiconducteur (4) et par une électrode inférieure formée par la partie de caisson (32) ; et la partie de caisson étant disposée de façon à être polarisée avec une tension située à un niveau intermédiaire entre une première tension de stockage et une seconde tension de stockage appliquée à la couche de semiconducteur, réduisant de ce fait l'intensité du champ établi dans le diélectrique de la capacité de la cellule mémoire.

2. Dispositif de mémoire semiconducteur selon la revendication 1, dans lequel le transistor à effet de champ comprend une région de source (4s) et une région de drain (4d) formée dans la couche de semiconducteur (4) et une électrode de grille (6) formée dans une couche d'isolation de grille (5) formée sur la couche de semiconducteur (4).

3. Dispositif de mémoire semiconducteur selon la revendication 1 ou 2, dans lequel la capacité est une capacité du type en tranchée.

4. Dispositif de mémoire semiconducteur selon la revendication 3, dans lequel la couche de semiconducteur est composée d'une partie en

Fig. 1A

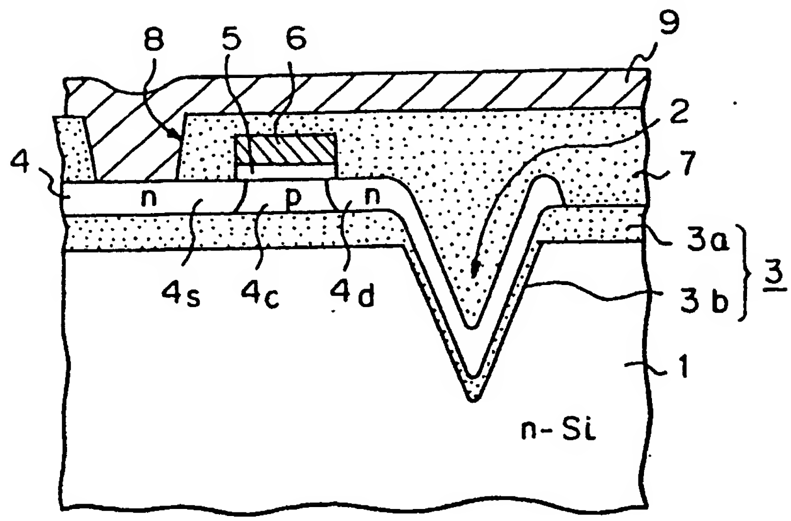

Fig. 1B

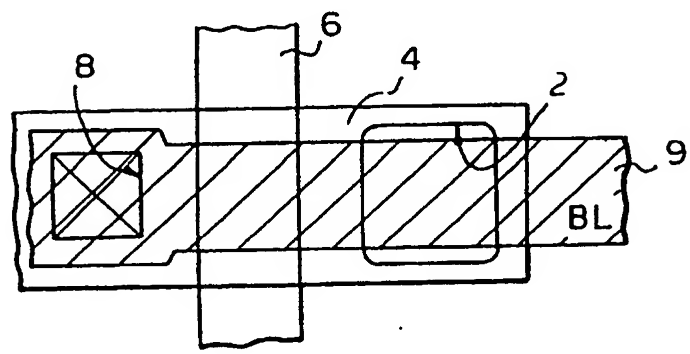

Fig. 3B Fig. 3A

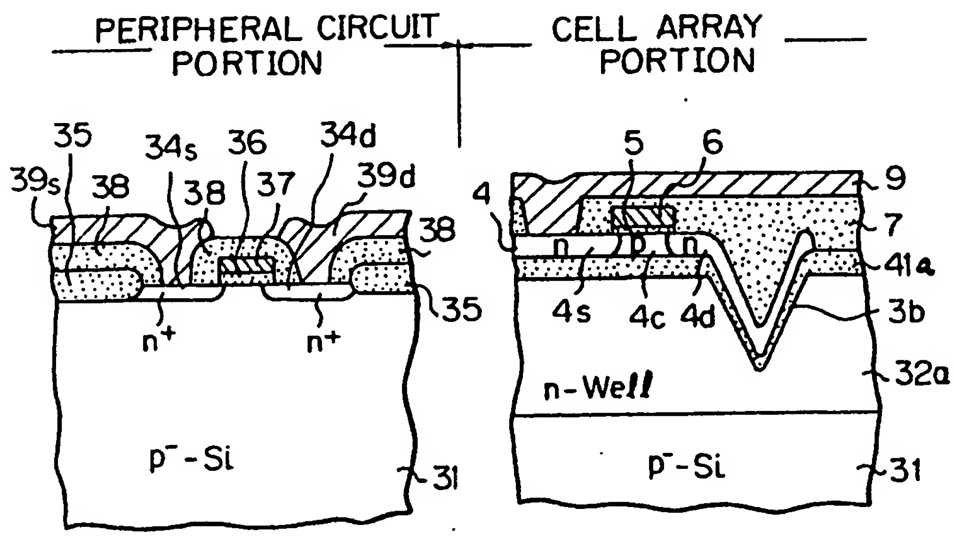

Fig. 3C